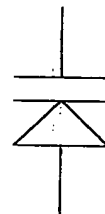
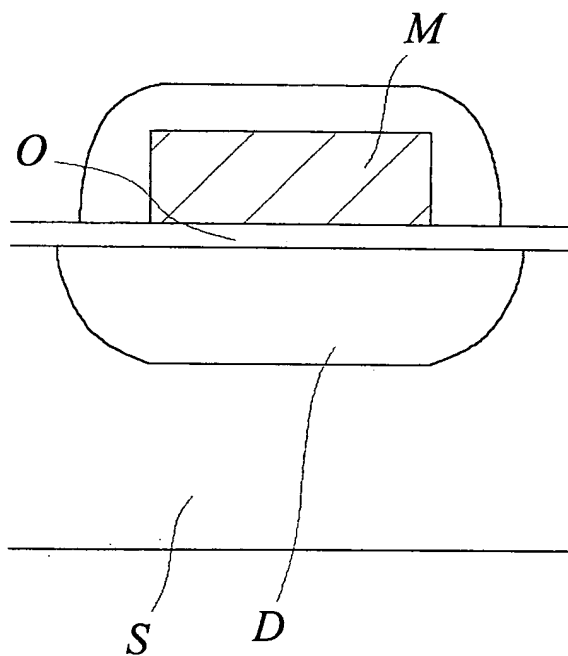
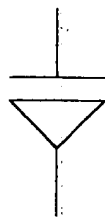


*FIG. 1(a) MOS capacitor*      *FIG. 1(c)*



*FIG. 1(d)*



*FIG. 1(b) MOS cap C-V relation*

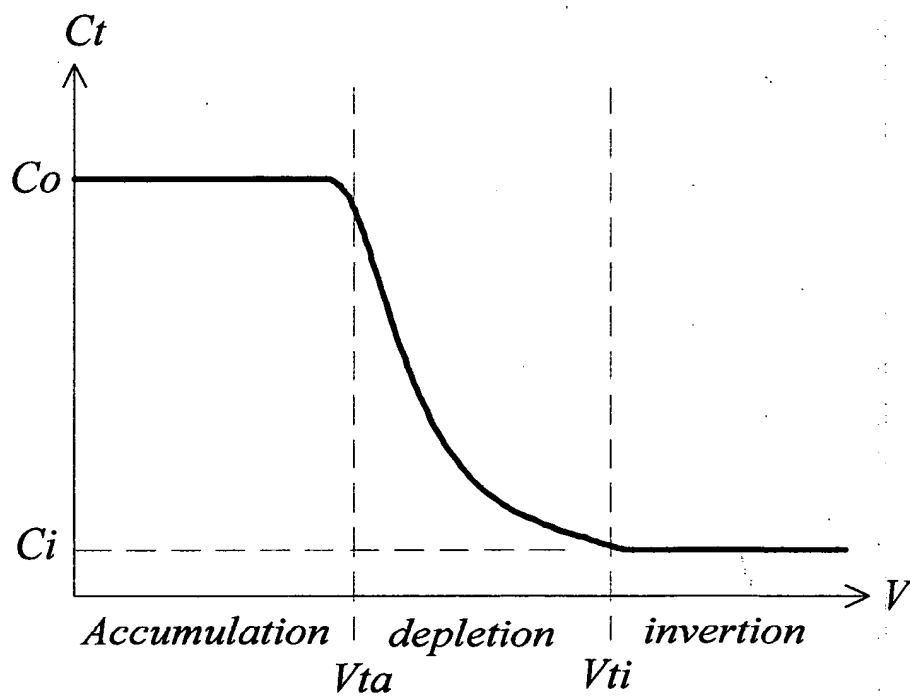


FIG. 2(a) FG capacitor

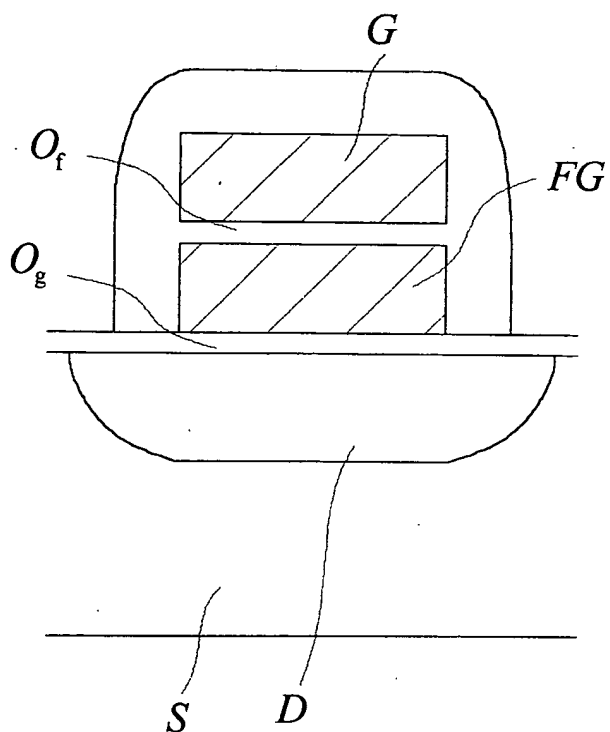


FIG. 2(c)



FIG. 2(d)

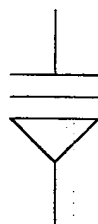


FIG. 2(b) FG C-V relation

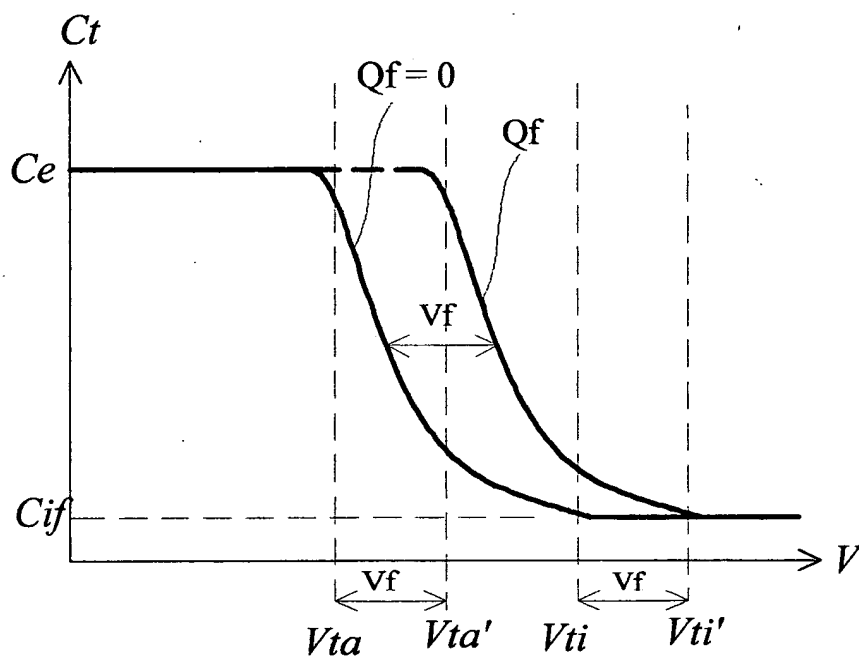


FIG. 3(a) prior art PLA minterm

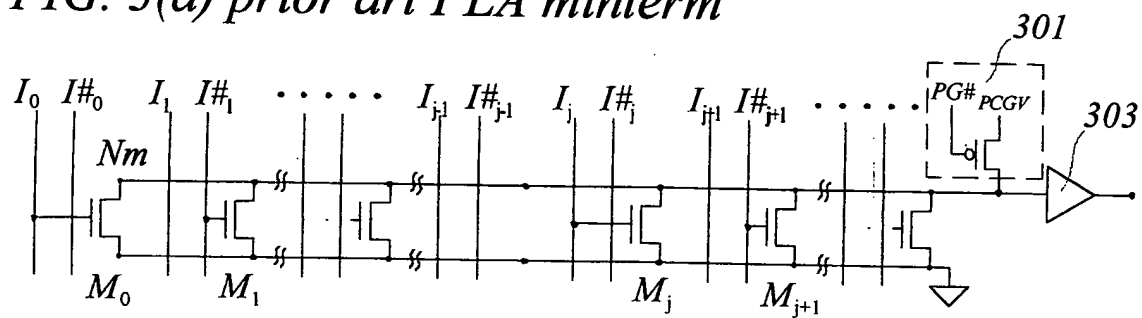


FIG. 3(b) prior art PLA operation

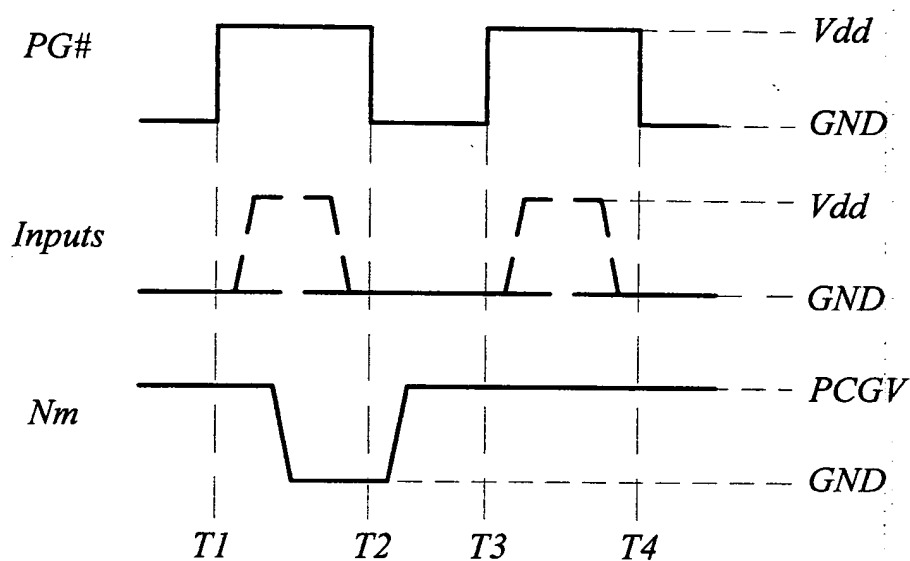


FIG. 4(a)

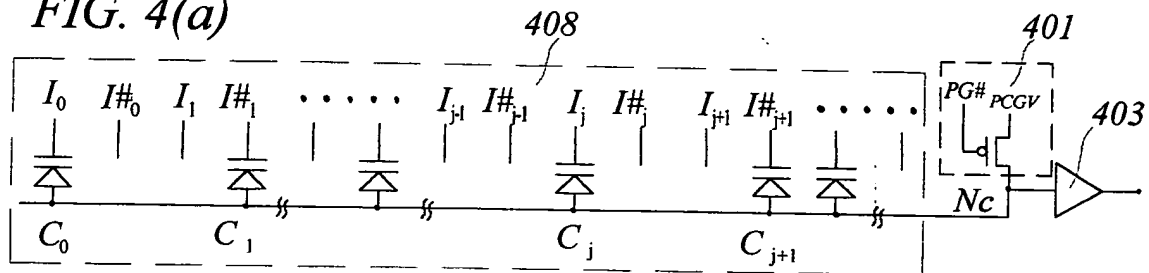


FIG. 4(b)

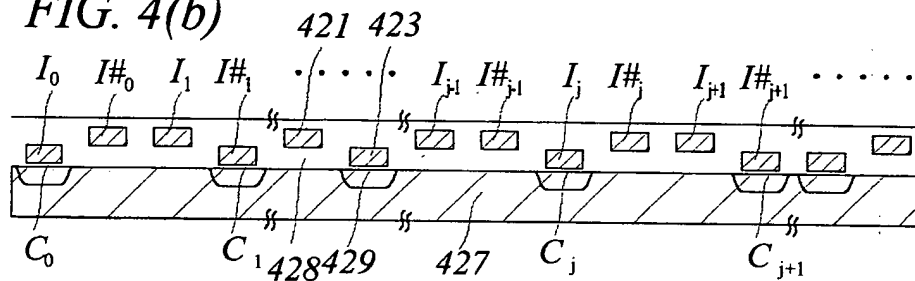


FIG. 4(c)

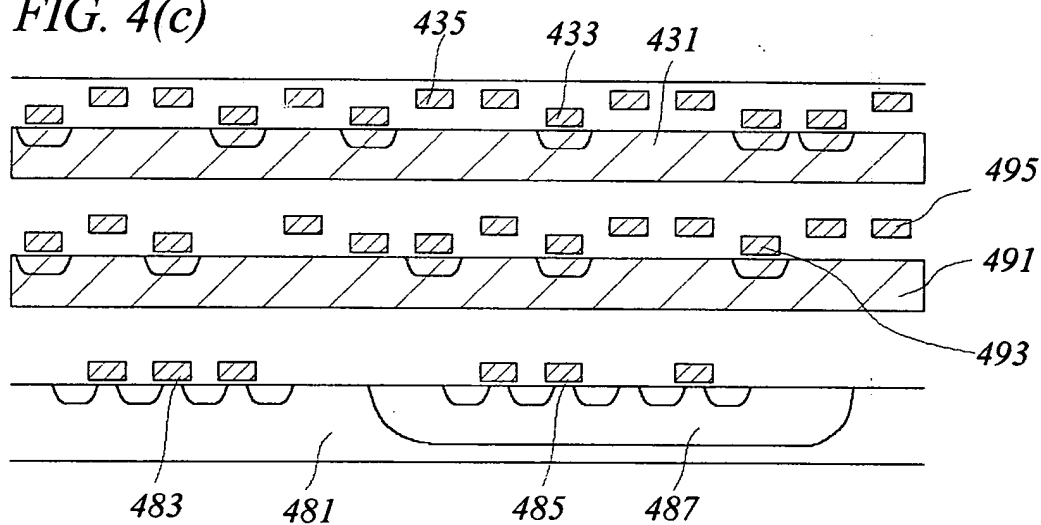


FIG. 4(d)

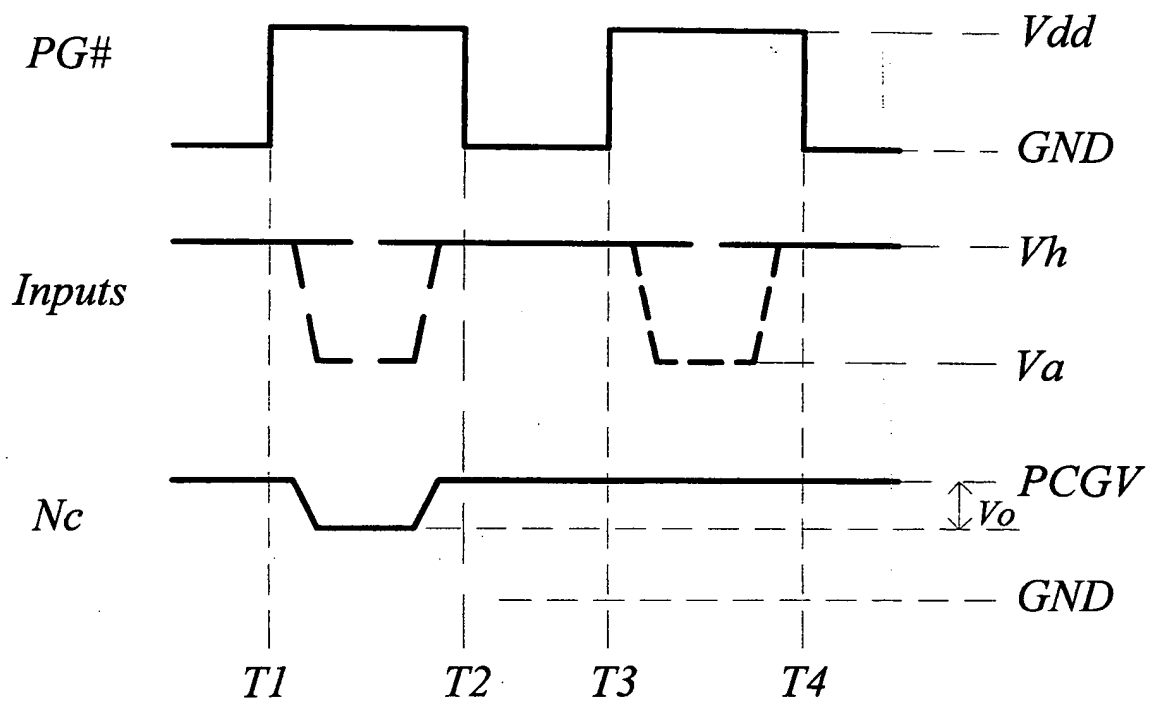


FIG. 4(e)

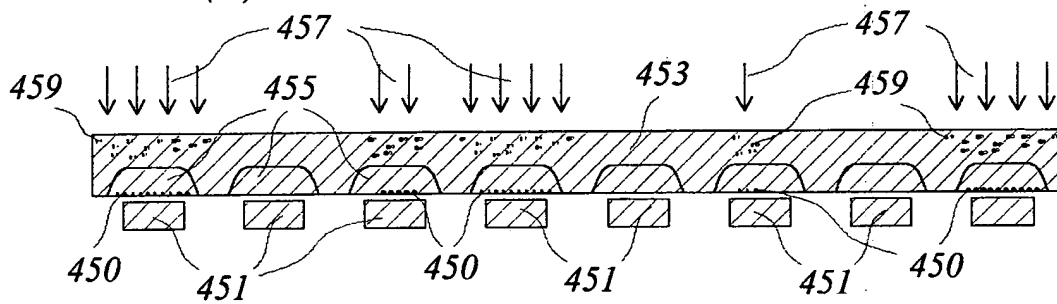


FIG. 5(a)

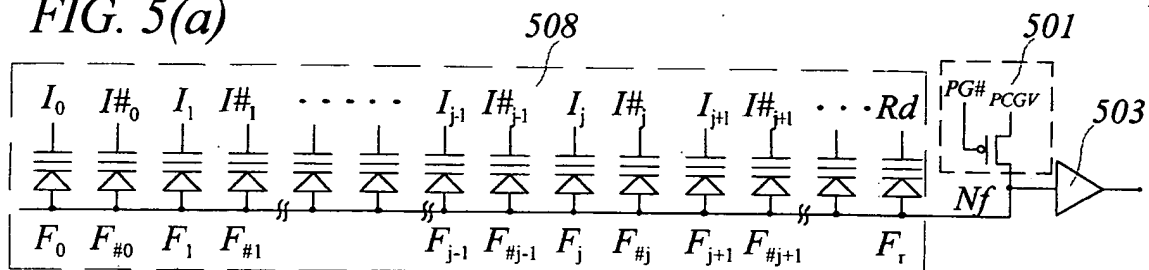


FIG. 5(b)

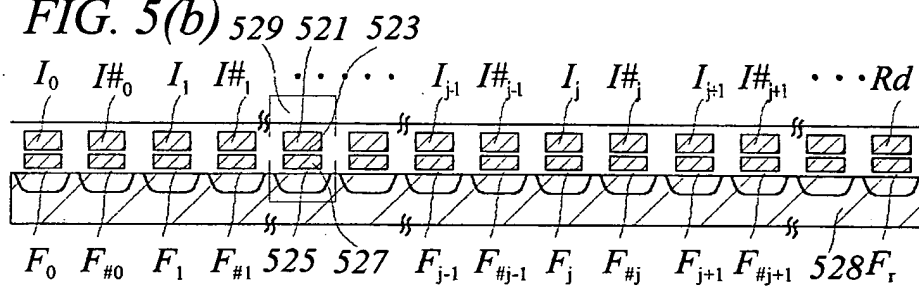
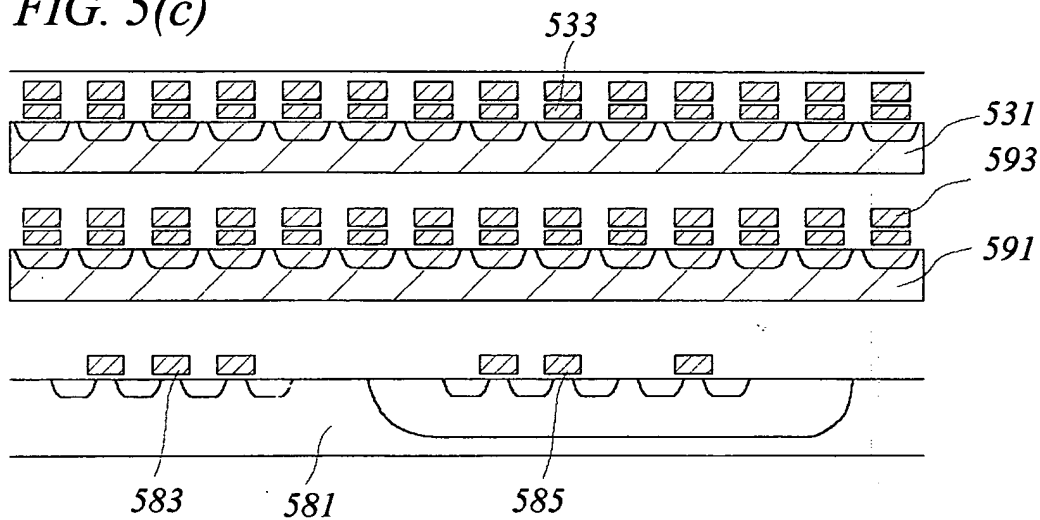


FIG. 5(c)



*FIG. 5(d)*

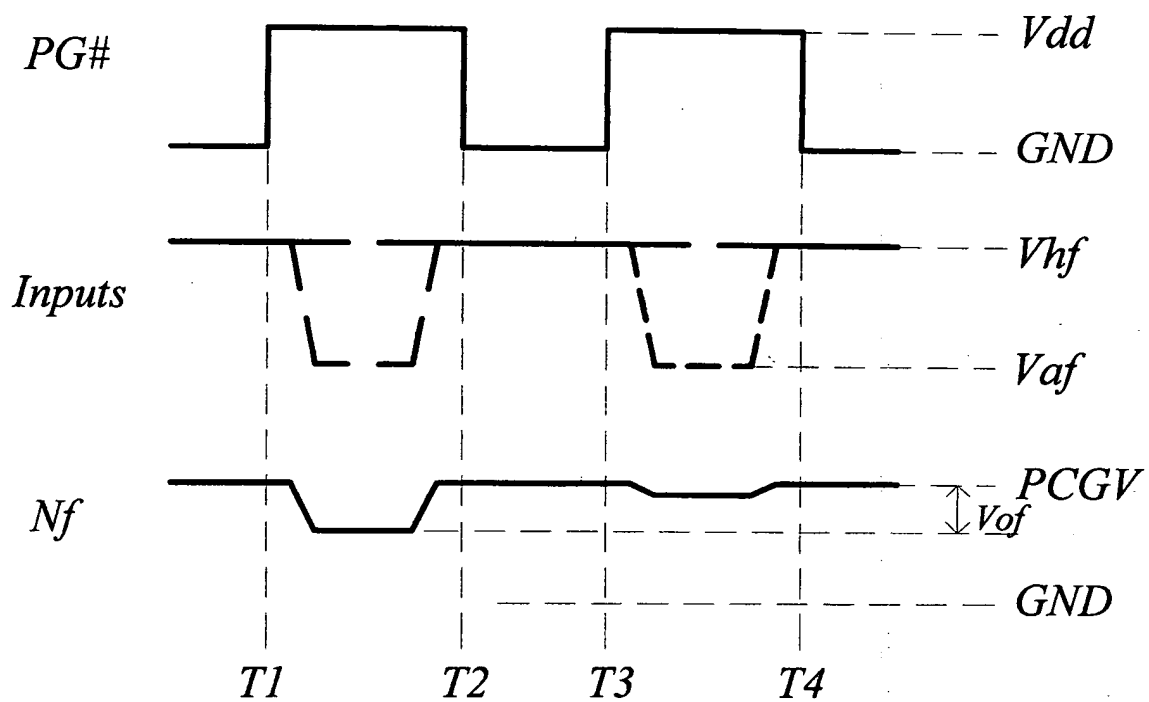


FIG. 5(e)

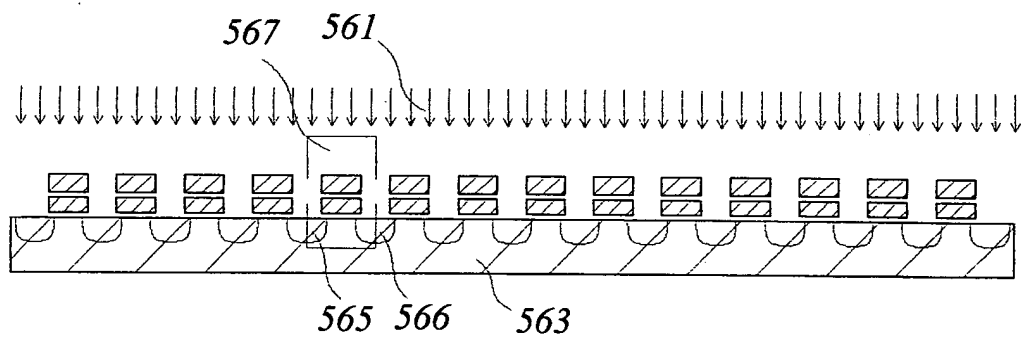


FIG. 5(f)

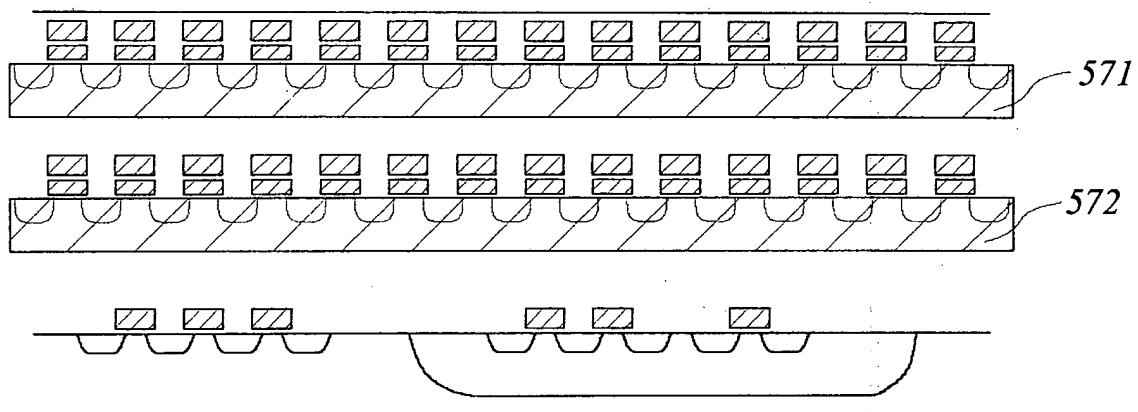




FIG. 6(a)

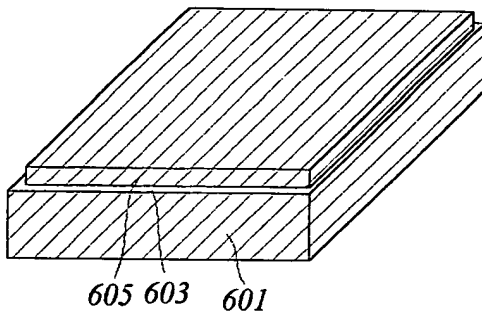


FIG. 6(b)

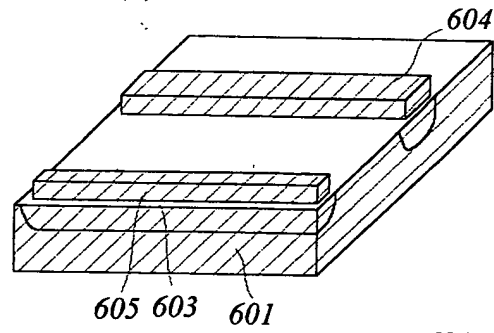


FIG. 6(c)

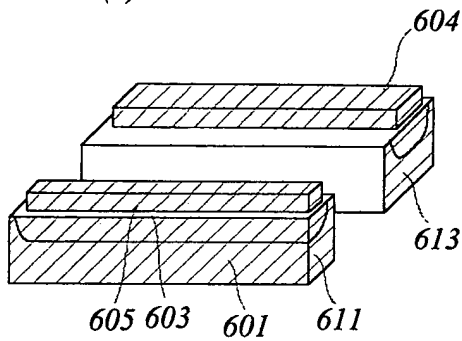


FIG. 6(d)

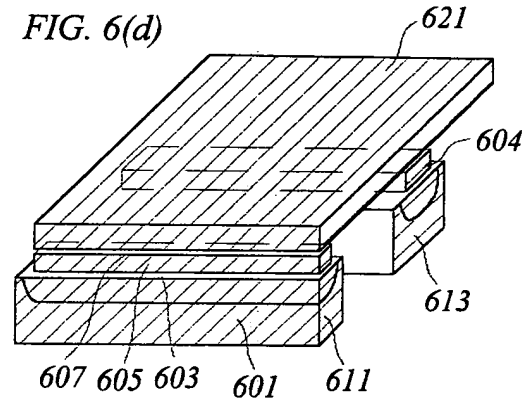


FIG. 6(e)

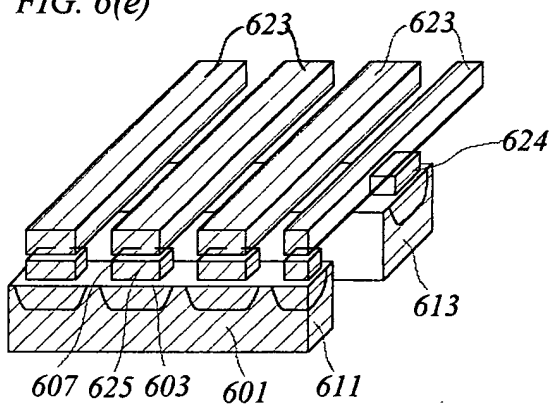


FIG. 6(f)

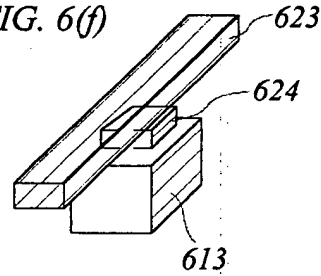


FIG. 6(g)

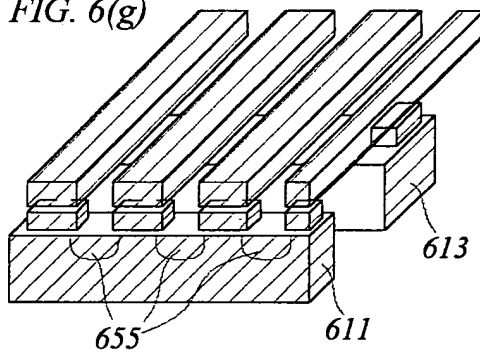


FIG. 7(a)

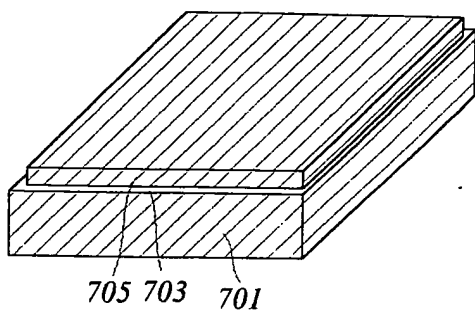


FIG. 7(b)

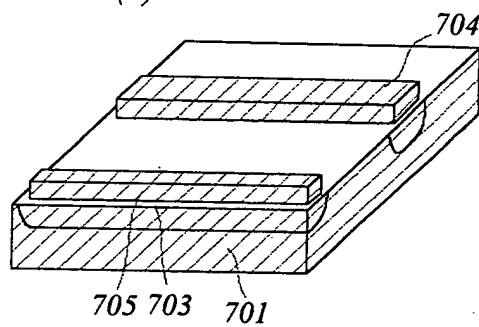


FIG. 7(c)

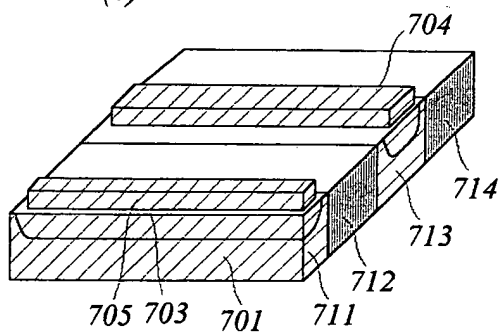


FIG. 7(d)

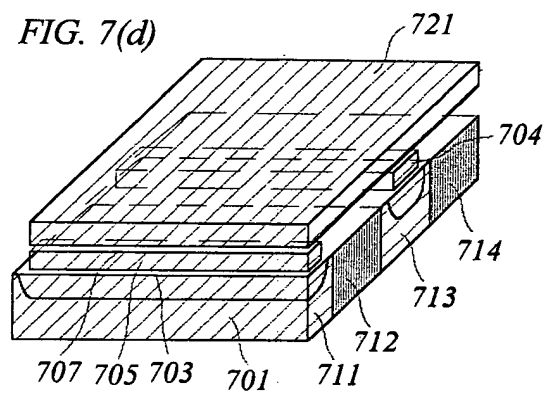


FIG. 7(e)

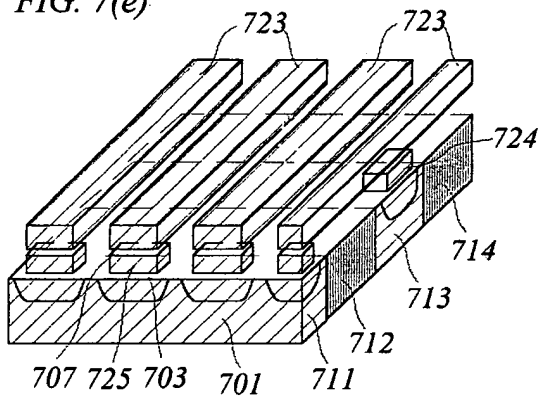


FIG. 7(f)

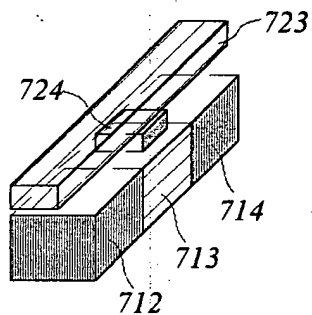


FIG. 8(a)

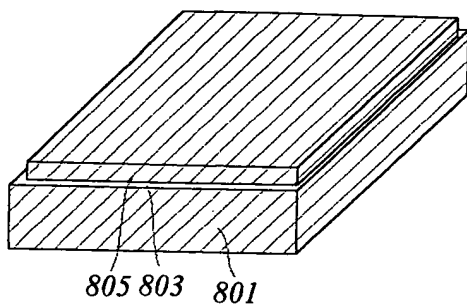


FIG. 8(b)

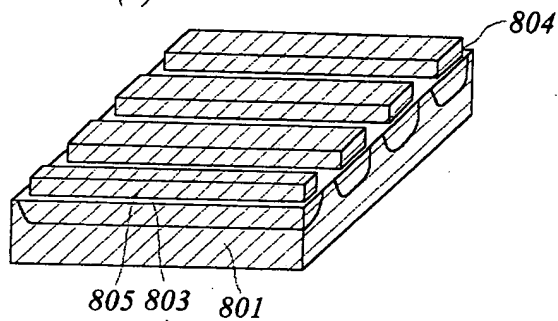


FIG. 8(c)

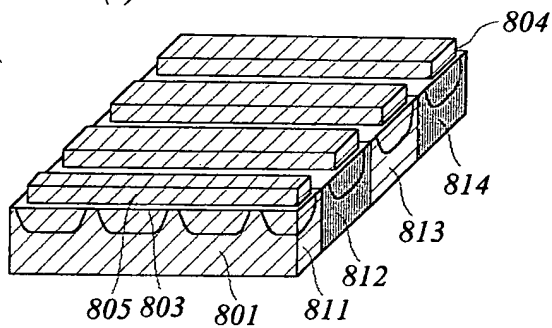


FIG. 8(d)

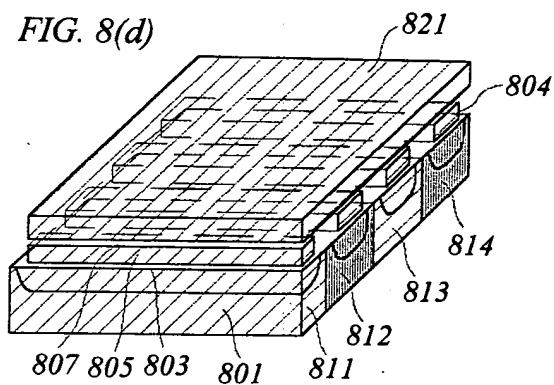


FIG. 8(e)

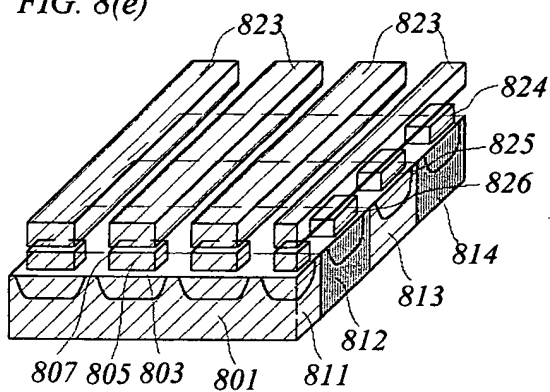
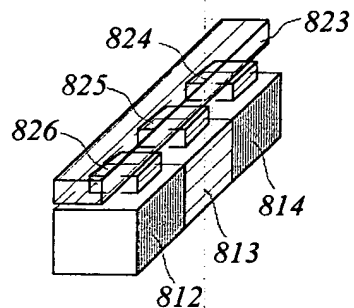
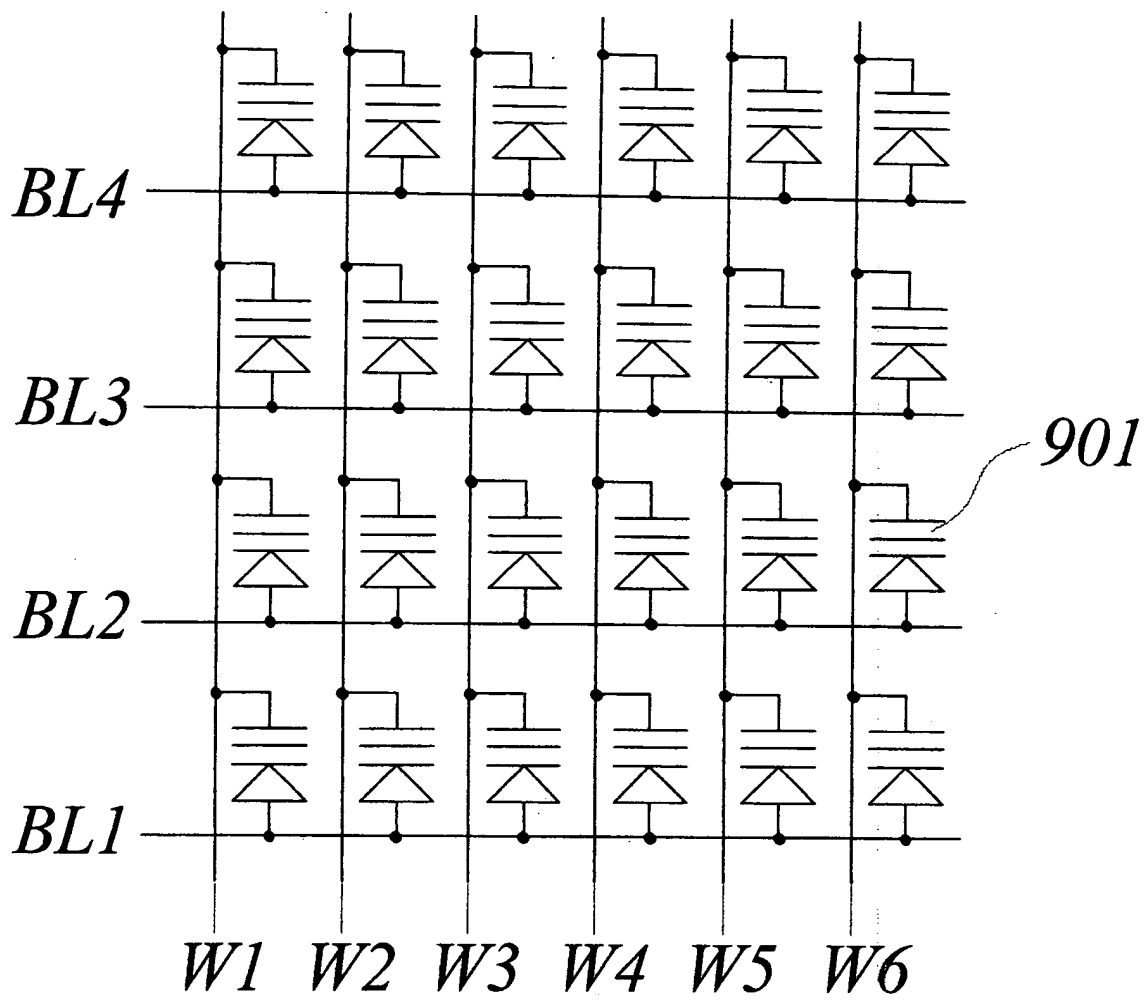


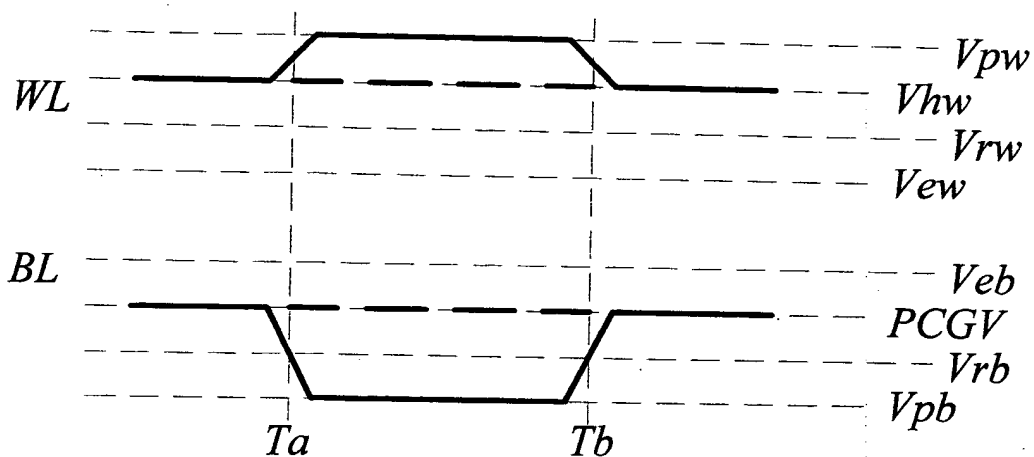
FIG. 8(f)



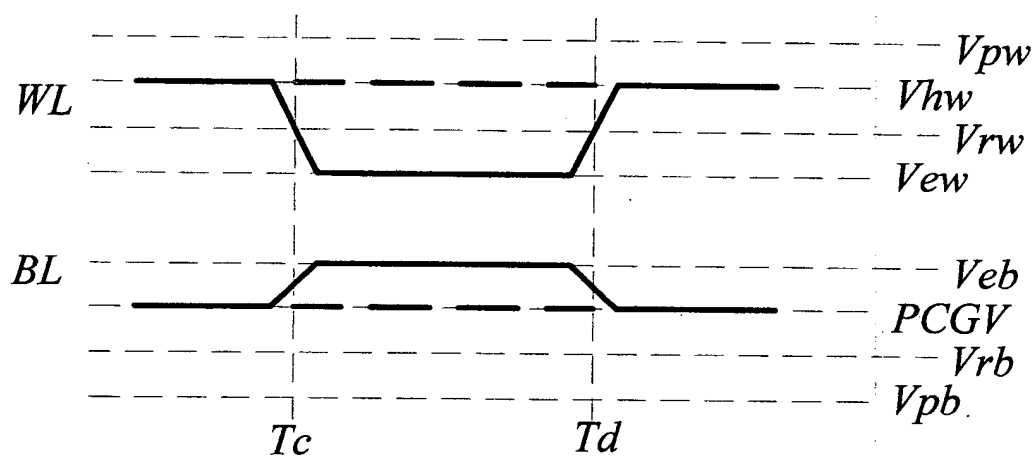
*FIG. 9(a)*



*FIG. 9(b) program*



*FIG. 9(c) erase*



*FIG. 9(d) read*

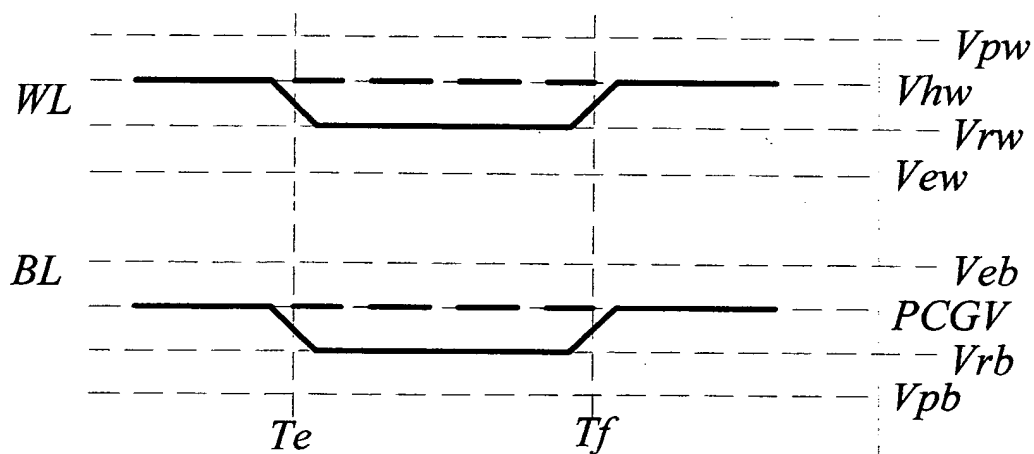


FIG. 9(e)

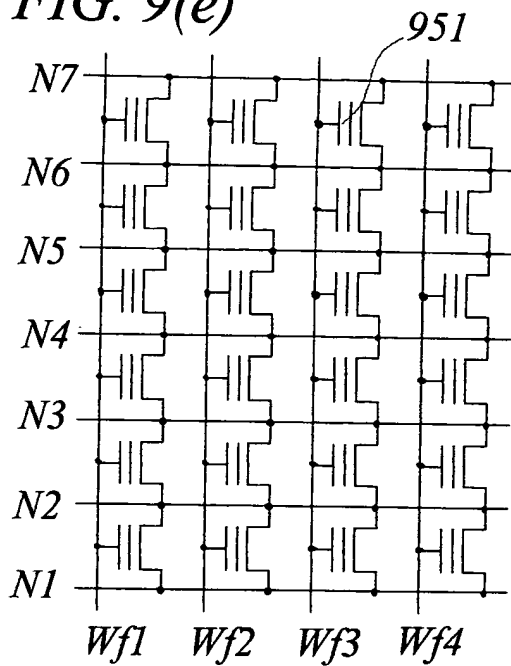


FIG. 9(f)

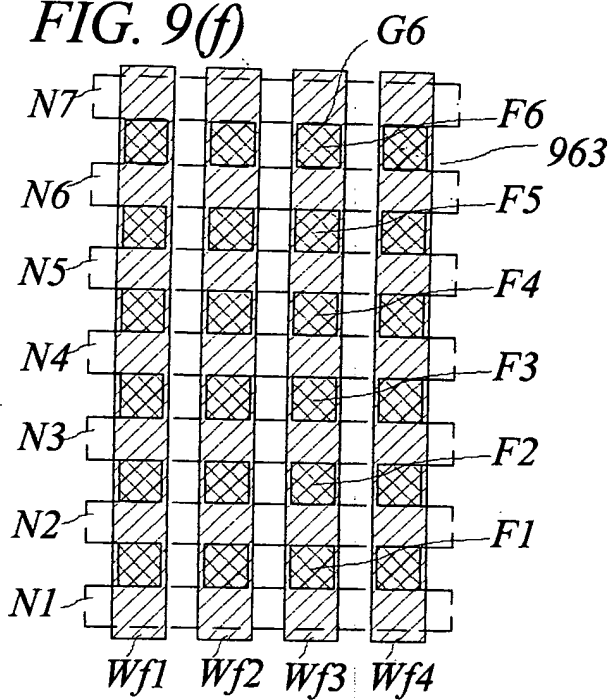


FIG. 9(g) prior art NOR FLASH array

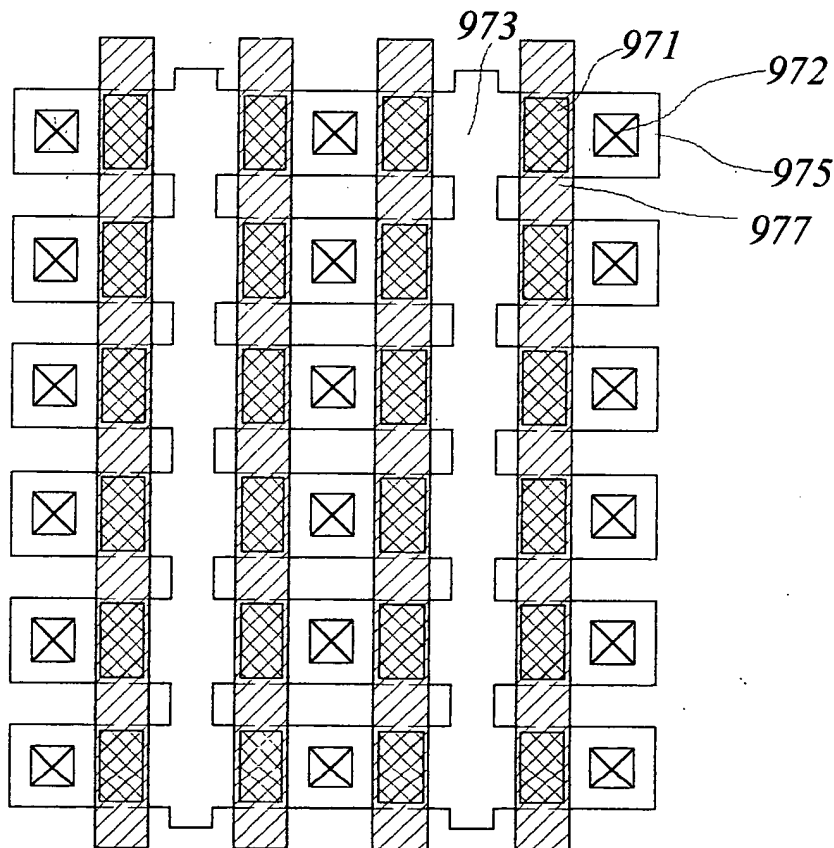


FIG. 10

